Current-Mode Analog Multiplier Based on Trasnlinear Loops

by

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Abstract

A wide range, Current mode four quadrant Analog Multiplier based on Tranlinear Loops is proposed in this work. The proposed multiplier is designed in 65nm technology using CMOS transistors operating in weak inversion. A thorough analysis of the proposed design is performed using Spectre and monte-carlo simulations. The multiplier consumes a low power of $0.6\mu W$ and supports an input range of $\pm 200nm$ while operating from 0.8V supply. The proposed multiplier exhibits an average Total Harmonic Distortion of 1.42% across different process and mismatch corners.
Chapter 1

Introduction and Overview

1.1 Background and Motivation

The evolution of integrated circuit technology and future scenarios of ubiquitous and pervasive computing have stressed the need for very low power and low voltage circuits with high signal density range and high linearity. The same can be applied to Analog Multipliers, which have found its application as programming element in systems such as filters [5], phase detection [6], neural networks [7], sensor applications [8], gain controlling [9], fuzzy systems [10] and as mixers [11] and modulators in a communication system.

While analog multipliers have been around for a long time, there is a recent increase in research attention on low power, low voltage current-mode circuits. This research attention has been mainly driven by the need to have low power and small area analog computing systems that can be used for machine learning and hardware security applications.

The increasing demand for low voltage/low-power integrated circuits has encouraged the development for CMOS current mode architecture. In current mode circuits the input and output signals are currents, the circuit performance is fully determined by currents and the voltage levels are irrelevant in determining the circuit performance. Moreover, in current mode circuits high gain is mostly not required. This results in simpler hardware structures. This justifies the growing range of applications of current mode circuits; for example in neural networks, microwave and optical systems, continuous time filters and sampled data filters.

In addition, having the transistors in weak inversion region adds up to reduction in power dissipation. Besides low power consumption, in weak inversion the gm/IDS value (i.e. the efficiency of the transistor) at a given bias current is the maximum available.

In this perspective, a current mode Analog multiplier based on Translinear Loops carries the advantages mentioned above.

1.2 Analog Multipliers

The history of analog multipliers originated from its use a mixer and as an amplitude modulation, which involves multiplication of two signals. Multipliers perform linear product if two signals \( x \) and \( y \) yielding an output \( z = Kxy \), where \( K \) is a multiplication constant.
Chapter 1 Analog Multipliers

Figure 1.1: Basic Idea of Multiplier [1]

with suitable dimension. Multipliers are often categorized as single-quadrant, where x and y are unipolar, two quadrant, with either x or y being unipolar and four-quadrant, where both x and y can be unipolar.

Fig.1.1 [1] illustrates the basic idea of the multiplier implementation. Two signals, \( v_1(t) \) and \( v_2(t) \), are applied to a nonlinear device, which can be characterized by a high order polynomial function. This polynomial function generates terms like \( v_1^2(t) \), \( v_2^2(t) \), \( v_1^3(t) \), \( v_2^3(t) \), \( v_1^2(t)v_2(t) \) and many others besides the desired \( v_1(t)v_2(t) \). Then it is required to cancel the undesired components. This is accomplished by a cancellation circuit configuration.

A multiplier could be realized using programmable transconductance components. Consider the conceptual transconductance amplifier of Fig.1.2a, where the output current is simply given by

\[
i_o = G_{m1}v_1
\]  

(1.1)

where

\[
G_{m1} = G_{m1}(I_{bias1})
\]  

(1.2)

For a bipolar transconductance, \( G_{m1} \) becomes

\[
G_{m1} = \frac{I_{bias1}}{2V_t}
\]  

(1.3)

where \( V_t \) is the thermal voltage \( (kT/q) \).

Next, a small signal \( i_2 \) is added to the bias current as shown in Fig.1.2b. The second input signal \( v_2(t) \) can be converted into a current, \( i_2(t) = G_{m2}v_2(t) \) as illustrated in Fig.1.2c. Then, the output current yields

\[
i_o = G_{m1}v_1 = \frac{I_{bias1} + G_{m2}v_2(t)}{2V_t}v_1(t)
\]  

(1.4)

\[
i_o = \frac{G_{m2}v_1(t)v_2(t)}{2V_t} + \frac{i_{bias1}v_1(t)}{2V_t}
\]  

(1.5)

or

\[
i_o = \frac{I_{bias2}v_1(t)v_2(t)}{2V_t2V_t} + \frac{I_{bias1}v_1(t)}{2V_t}
\]  

(1.6)

or

\[
i_o = 2k_1v_1(t)v_2(t) + k_2v_1(t).
\]  

(1.7)
Thus, \( i_o(t) \) represents the multiplication of two signals \( v_1(t) \) and \( v_2(t) \) and an unwanted component \( k_2 v_1(t) \). This component can be eliminated as shown in the Fig.1.2d. Better cancellation is achieved when third transconductor \( G_{m2} \) becomes a fully differential transconductor, and \( v_1 \) and \( v_2 \) are fully differential inputs as illustrated in Fig.1.2e.

\[
    i_o = 2k_1 v_1(t) v_2(t)
\]

This is the basic principle of a Gilbert cell [12]. The connection to the Gilbert cell can be seen by substituting the transconductors in Fig. by bipolar Junction transistors (BJT) differential pairs.
Chapter 2

CMOS Transconductance Multipliers

2.1 Operation Modes and Circuit Topologies

In the paper [1], the author had made efforts to classify transconductance multiplier into eight types. They can be grouped into two groups based on its MOS operating region, linear and saturation. It should be emphasized that the fundamental multiplier circuit topology for many of the multipliers is the same. Besides the above major multiplier structures, multipliers operating in the weak inversion region, dynamic multiplier for sampled signal system or neural networks, voltage-current, and current-current multipliers have been reported.

Despite many reported circuits, only two cancellation methods for the four-quadrant multiplication are known. Since a single-ended configuration cannot achieve complete cancellation of nonlinearity and has poor power supply rejection ratio (PSRR), a fully differential configuration is necessary in a sound multiplier topology. The multiplier has two inputs, therefore there are four combinations of two differential signals, i.e., \((x, y), (-x, y), (-x, -y), (x, -y)\). The topology of Fig. 2.1a is based on single quadrant multipliers. Fig. 2.1b is based on square law devices. These topologies achieve multiplication and simultaneously cancel out all the higher order and common mode components (X and Y) based on the following equalities:

\[
[(X + x)(Y + y) + (X - x)(Y - y)] - [(X - x)(Y + y) + (X + x)(Y - y)] = 4xy
\]  

(2.1)

or

\[
\left\{(X + x) + (Y + y)\right\}^2 + \left\{(X - x) + (Y - y)\right\}^2 - \left\{(X - x) + (Y + y)\right\}^2 - \left\{(X + x) + (Y - y)\right\}^2 = 8xy
\]  

(2.2)

MOS transistors can be used to implement these cancellation and because the MOSFET is a transconductance device, the fundamental operation is a transconductance multiplier. The simple MOS transistor model can be expressed as

\[
I_d = k\left[V_{gs} - V_T - \frac{V_{ds}}{2}\right]V_{ds} = K\left[V_{gs}V_{ds} - V_T V_{ds} - \frac{V_{ds}^2}{2}\right], \text{for } V_{gs} > V_T, V_{ds} < V_{gs} - V_T
\]

(2.3)
Chapter 2

Multipliers Operating in Linear

(a) Using Single-Quadrant Multipliers
(b) Using Square Devices

Figure 2.1: Four-Quadrant Multipliers Basic Architectures [1]

\[ I_d = \frac{K}{2} [V_{gs} - V_T]^2 = \frac{K}{2} [V_{gs}^2 - 2V_{gs}V_T - V_T^2], \text{for } V_{gs} > V_T, V_{ds} > V_{gs} - V_T \] (2.4)

for NMOS, in its linear and saturation region respectively. \( K = \mu_o C_{ox} \frac{W}{L} \) and \( V_T \) are the conventional notation [13] for the transconductance parameter and the threshold voltage of the MOS transistor respectively. The terms \( V_{gs}V_{ds} \) in (2.3), \( V_{ds}^2 \) in (2.3), or \( V_{gs}^2 \) in (2.4) can be used to implement (2.1) and (2.2), respectively.

Fig.2.2 shows the application methods for two signals (x and y) in a MOSFET. x and y are time-variable voltage signals, disregarding the bias. The first three methods (2.2a, 2.2b and 2.2c) are used for FET’s operating in their linear region and the rest are for the transistors operating in saturation. The signal injection methods (2.2b), (2.2d) and (2.2g) require a voltage summing circuits, which can be implemented in many different ways [14]-[15].

The next two sections discusses about few models, which have been categorized based on MOS operating regions as mentioned above.

2.2 Multipliers Operating in Linear

Before going into further discussion, it is important to know about a programmable linear transconductor and its working. Using two of these, a multiplier can be realized. Shown in the figure Fig.2.3 is a programmable transconductor [16].

When proper bias voltage X and Y are given, \( M_1 \) operates in linear region and \( M_s \) operates in saturation region. If the transconductance of \( M_s(K_2) \) is much larger than transconductance of \( M_1(K_1) \), then \( M_s \) behaves as source follower and \( V_{ds} \) of \( M_1 \) is controlled by y through the source follower \( M_s \). A BJT emitter follower [17] [Fig.2.3b] or a gain enhanced MOS source follower [18]-[19], can be used to replace the \( M_s \) in Fig.2.3a. The configuration shown in Fig.2.3c is used to enhance the effective transconductance of the
source follower. An improper design of amplifier $A$, may cause some stability problem in the gain-enhanced MOS source follower.

Now that we have discussed about the programmable transconductors, combining two of these as shown in the Fig.2.4a will give us one of the multiplier models. Using equation 2.3 and replacing $V_{gs}$ and $V_{ds}$ by $X \pm x$ and $y$, we can get the output currents, as

$$I_1 = K \left( X + x - V_T - \frac{y}{2} \right) y$$

$$I_2 = K \left( X - x - V_T - \frac{y}{2} \right) y$$

(2.5)

The difference of the output currents yields a multiplication as

$$I_0 = I_1 - I_2 = 2Kxy$$

(2.6)

The configuration in Fig.2.4b, uses MOS source followers and achieves multiplication in the same way in (2.5) except $y$ in (2.5) is replaced with $Y \pm y - V_T$

The configuration shown in the figure Fig.2.5 a fully differential configuration using four MOS transistors operating in linear region. Using this configuration improves the linearity and PSRR because a better nonlinearity cancellation is obtained. These configurations are based on the topology in Fig1.2b and corresponds to (2.1), yielding

$$I_o = I_{o1} - I_{o2} = \left( I_1 + I_3 \right) - \left( I_2 + I_4 \right) = 4Kxy$$

(2.7)

or

$$V_o = -Z_f I_o = -4KZ_fxy$$

(2.8)
Chapter 2

Multipliers Operating in Linear

Figure 2.3: Programmable Transconductors

Figure 2.4: Four-Quadrant Multipliers with Two Transistors Operating in Linear Region [1]

The op amp in Fig. 2.5a [20–22] can be replaced by the source followers shown in the Fig. 2.5b [23]. This is possible because the purpose of the op amp is to keep the source potential of transistors constant.

The MOSFET operating in the linear region has a square term, $V_{ds}^2$ as in 2.3. This term forms the basis of the next model in discussion. Using this, we can realize the cancellation method in 2.2.

In the model shown in the figure Fig. 2.6, sum and the difference of two input signals are applied to the gate of the source followers, $M_s$, and they control the drain voltage of $M_1$ that operates in the linear region. The summer indicated in at the gate of the $M_s$ can be implemented using an active circuitry or passive components such as resistors or a floating gate [14]. This circuit based on 2.2, yields

$$I_o = I_{o1} - I_{o2} = Kxy$$

The major disadvantage of this configuration is having poor linearity.

The next model, uses modulation [24] to inject $V_{ds}$ signal. [Fig. 2.7]. The transistors $M_{d1}$ and $M_{d2}$ operate in saturation region while the others($M_1$, $M_2$) operate in saturation region.
Figure 2.5: Four-Quadrant Multipliers [1]

Figure 2.6: Multiplier Using $V_{ds}^2$ [1]
The output current of the circuit Fig.2.7b can be obtained as

\[ I_o = I_{o1} - I_{o2} = 8KV_{pol}C_{xy} \frac{x^2 + y^2 - 2C^2}{(4C^2 - (x + y)^2)(4C^2 - (x - y)^2)} \approx \frac{KV_{pol}}{C} x y \] (2.10)

where

\[ V_{pol} = \sqrt{\frac{I_{pol}}{K_d}} \text{ for } I_d \ll I_{pol} \] (2.11)

\[ C = V_{com} - V_s - V_T - V_{pol} \text{ and } C \gg x, y \] (2.12)

However this does not have clear advantage over other multiplier types.

For comparison purposes, the first model in this section is being tagged as Type 1, the second model as Type 2 and third one as Type 3.

2.3 Multipliers with Transistors Operating in Saturation Region

The first topology in this section is similar to Type 2 topology. The drain current of a diode connected MOSFET depends on \( V_{ds}^2 \) in the saturation region. Thus, the signal can be applied using source follower whose gate input is the sum and difference of two input signals as shown in Fig.2.8. The linearity of this configuration is often poorer.

The next topology is based on the Fig.2.1b, which is a four-quadrant Multiplier and can be realized by four cross-coupled transistors as shown in the Fig.2.9. This circuit yields an
output current of

\[ I_o = I_{o1} - I_{o2} = 4kxy \]  

(2.13)

based on 2.2 and 2.4. There are many varieties of source signal application methods, few of which are: Fig.2.10a uses and op amp [25], (2.10b) uses linear differential amplifier [26], (2.10c) uses source followers \( M_s \). A separate source follower as shown in Fig.2.10d, can be provided to each transistor in cross-coupled transistors [27]. This type is most widely implemented multiplier structure.

The third topology under this section uses the substrate terminal of the MOSFET. As long as the substrate-source junction is kept reverse biased, it can be used as an additional input terminal. The substrate potential controls threshold voltage for an NMOS transistor as

\[ V_T = V_{TO} + \gamma \left[ \sqrt{2|\phi_F|} - V_{bs} - \sqrt{2|\phi_F|} \right] \]  

(2.14)
where $V_{TO}$ is the threshold voltage when $V_{bs} = 0$, $\gamma$ is the body effect coefficient, and $\phi_F$ is the Fermi potential. Substituting $V_T$ in 2.4 with 2.14, the configuration shown in 2.11, based on the topology Fig.2.1b and 2.4, gives

$$I_o = 4K\gamma / \phi_F - Y + s \approx 4K\gamma / \phi_F - Y + s$$

(2.15)

The approximation is valid only if $2|\phi_F| - Y + s \gg y$

The last topology to be discussed in this section is based on the nonlinearity cancellation of Fig.2.1b and voltage summing circuits. Four cross-coupled transistors with voltage summer realize a four quadrant multiplier as shown in the Fig.2.12a. The Fig.2.12b shows the same circuit without tail current. The output current is obtained as

$$I_o = 4KK_a xy$$

(2.16)

based on (2.2) and (2.4).

This configuration is reported in [28–30] using a capacitive adder, in [31] using a resistive adder, and in [19,32,33] using an active adder.

Reference [34] provides a summary of this multiplier. The structure of this topology is similar to the first topology in this section. As the previous one requires an additional transistor, it does not have any advantage over this.
For convenience in comparison, the topologies mentioned in this section are tagged as type 4, type 5, type 6 and type 7 in the respective order of their mention in this section.

In [1], the author tabulated the general comparison of the multiplier topologies discussed above. The table is as presented below
## Chapter 2 Multipliers with Transistors Operating in Saturation Region

<table>
<thead>
<tr>
<th>NO</th>
<th>Type</th>
<th>Circuit Diagram Figure</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>2.5a, 2.5b</td>
<td>Require additional circuitry</td>
</tr>
<tr>
<td>2</td>
<td>2, 3, 4</td>
<td>2.6, 2.7, 2.8</td>
<td>Requires additional Circuitry. Poor linearity</td>
</tr>
<tr>
<td>3</td>
<td>5</td>
<td>2.10a</td>
<td>Require Op Amp</td>
</tr>
<tr>
<td>4</td>
<td>5</td>
<td>2.10b, 2.10c, 2.10d</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>6</td>
<td>2.11</td>
<td>Poor Linearity</td>
</tr>
<tr>
<td>6</td>
<td>7</td>
<td>2.12</td>
<td>Require additional circuitry</td>
</tr>
</tbody>
</table>

Table 2.1: SUMMARY OF GENERAL COMPARISON OF MULTIPLIER TOPOLOGIES [1]
Chapter 3

Low-Voltage Analog Multipliers

3.1 Current Mode Circuits

The information processed by lumped electric networks can be represented by either the nodal voltages or branch currents of the networks. The former are referred to as voltage-mode circuits whereas the latter are known as current-mode circuits. Together, they provide a complete characterization of the behavior of the networks.

Voltage-mode circuits have received a much broader attention and found a much wider range of applications as compared with their current mode counterparts despite the fact that the concept of ideal current mode circuits, similar to that of ideal voltage-mode circuits, emerged approximately 40 years ago. This is reflected by a handful monographs on current-mode circuits but countless texts on voltage mode circuits. The reasons for such a popularity that voltage-mode circuits have been enjoying can be summarized as follows:

1. The nodal voltage of electric networks can be measured conveniently using voltmeters without modifying the topology and affecting the operation of the networks. On the contrary, the measurement of the branch current of the networks are less convenient and often requires a change of the configuration of the networks or additional circuitry,

2. The infinite impedance looking into the gate of MOS transistors makes these devices an ideal choice for the realization of voltage-mode circuits, especially in cascade configurations, such as multi-stage voltage amplifiers

3. The ease to obtain a high voltage gain of voltage-mode circuits using techniques such as cascodes and regulated cascodes.

4. High supply voltages available in the past such that low-voltage design was not of a critical concern

5. Switching noise was not a critical issue with the presence of a high supply voltage

6. Low speed requirements permit the charge and discharge of nodal capacitors over a long period of time

The aggressive reduction in the supply voltage and the moderate reduction in the device threshold voltage of CMOS technology have greatly affected the performance of CMOS
Chapter 3  MOS Translinear Principle

voltage-mode circuits, typically reflected by a reduced dynamic range, an increased propagation delay, and reduced low noise margins. The impact of supply voltage reduction on the performance of current-mode circuits, however, is less severe as compared with that of voltage-mode circuits. This is because the design emphasis of current-mode circuits is on branch currents rather than nodal voltages. The usefulness of CMOS current-mode circuits in combating the difficulties arising from the reduction of the supply voltage and the increase in the operation speed has received an increasing attention both from industry and academia recently. The different design focuses of voltage-mode and current-mode circuits, arising from the intrinsic characteristics of nodal voltages and branch currents, result in distinct design principles.

3.2  MOS Translinear Principle

Translinear principle, first introduced by Gilbert in 1975, is one of the most important contributions to the circuit theory in electronics era [35]. In its basic definition, the translinear principle provides a simple and efficient way to analyze and synthesize linear circuits based on bipolar junction transistors. Due to their exponential characteristics, the translinear principle can be extended to MOS transistors operating in weak inversion region [36].

In contrast, the translinear principle holds for MOS subthreshold transistors in an exact manner if source and bulk are short circuited. However, it has been found that the principle holds as well in an exact manner under different circumstances [36, 37]. In the paper [38], a general theorem and the conditions under which subthreshold MOS transistors, satisfy a general translinear principle has been defined.

The operation of subthreshold MOS can be described by the following equation [36], [38]:

\[
I_{DS} = I_o \frac{W}{L} e^{\kappa(V_{GS}/V_{th})} e^{(1-\kappa)(V_{BS}/V_{th})} \left(1 - e^{-V_{DS}/V_{th}}\right) \tag{3.1}
\]

where \(V_{th} = KT/q\) is the thermal voltage, \(I_o\) is a positive constant current, \(W\) is transistor width and \(L\) is its length, and \(\kappa\) is a technology dependent positive parameter. This equation holds good as long as

\[
\frac{1}{2} \phi_{FB} \leq V_{GS} \leq \phi_{FB} \tag{3.2}
\]

where \(\phi_{FB}\) is the device’s flat band voltage [39]. Voltage \(V_{BS}\) can take either positive or negative values as long as the parallen PN diode junction is biased below its forward conduction threshold voltage. Parameter \(\kappa\) is known to have slight dependency on voltage \(V_{BS}\), however, if care is taken to make the \(V_{BS}\) voltages similar for all transistors, \(\kappa\) can be assumed to be constant.

For operation in saturation, (3.1) can be simplified to

\[
I = \frac{I_{DS}}{W/L} = I_o e^{\kappa(V_{GS}/V_{th})} e^{(1-\kappa)(V_{BS}/V_{th})}, \tag{3.3}
\]

if \(V_{DS} \gg V_{th}\)

where \(I\) is a transistor current normalized with respect to transistor size (W/L).

If \(V_{BS} = 0\) (or constant) there is an exact exponential relation between \(V_{GS}\) and \(I_{DS}\), 3.1 and the original BJT translinear formulation can be directly and exactly applied.
Chapter 3  

MOS Translinear Principle

Figure 3.1: Sub-Threshold MOS Transistors Translinear Loop [1]

The main principle of translinear says, that in a closed loop containing equal number of oppositely connected translinear elements, the product of the normalized currents in clockwise(CW) direction is equal to the corresponding product for the elements connected in counterclockwise(CCW) direction.

Using the circuit in Fig.3.1, let’s see how this happen. In, Fig.3.1, we have six transistors connected exactly as mentioned above. According Kirchoff’s law, in a loop, sum of branch voltages adds to zero. Since voltages of CW-oriented junctions have opposite sign than those of CCW-oriented junctions, the following holds:

$$\sum_{j \in (CW)} V_{GSj} - \sum_{i \in (CCW)} V_{GSi} = 0 \quad (3.4)$$

Since $V_{BS} = 0$ for all subthreshold MOS transistors, using 3.3 in 3.4 yields

$$\frac{V_{th}}{\kappa} \sum_{j \in (CW)} \ln \left( \frac{I_j}{I_o} \right) - \frac{V_{th}}{\kappa} \sum_{i \in (CCW)} \ln \left( \frac{I_i}{I_o} \right) = 0$$

$$\frac{V_{th}}{\kappa} \ln \left( \frac{\prod_{j \in (CW)} I_j}{\prod_{i \in (CCW)} I_i} \frac{\prod_{i \in (CCW)} I_o}{\prod_{j \in (CW)} I_o} \right) = 0$$

$$\frac{\prod_{j \in (CW)} I_j}{\prod_{i \in (CCW)} I_i} \frac{\prod_{i \in (CCW)} I_o}{\prod_{j \in (CW)} I_o} = 1 \quad (3.5)$$

Since the number of CW-oriented devices is equal to the CCW-oriented ones, the $I_o$ coefficients in 3.5 cancel out, thus resulting in

$$\prod_{j \in (CW)} = \prod_{i \in (CCW)} \quad (3.6)$$
3.3 Previous Architectures Related to Proposed Architecture

The proposed architecture uses MOSFETs which are in weak inversion region. So, this section presents few previous works, which used similar architecture for comparison purposes.

3.3.1 Low Power Four Quadrant CMOS Analog Multiplier/Divider (2005)

In the paper [2], a novel compact current mode CMOS four-quadrant analog multiplier using translinear loops [Explained in the Next Chapter] with MOS transistors operating in weak inversion region was presented.

In the Fig.3.2, the transistors $M_1, M_2, M_3 and M_4$, forming a translinear loop, implements the following operation: $I_{O1} = I^+_x I^+_w / I_B$. The transistors $M_7, M_8, M_11 and M_{12}$, forming a translinear loop, implements the following operation: $I_{O2} = I^-_x I^-_w / I_B$. The currents $I_{O1} and I_{O2}$ are summed at node n2, resulting in a positive single ended term of output current $I^{+}_{OUT}$:

$$I^{+}_{OUT} = I_{O1} + I_{O2} = \left( I^+_x I^+_w + I^-_x I^-_w \right) / I_B$$

(3.7)

In a similar way, the current term $I_{O3}$, (the result of the operation of the translinear loop made by the transistors $M_1, M_2, M_5 and M_6$) is summed at node n1 to the current term $I_{O4}$ (the result of the operation of the translinear loop made by the transistors $M_7, M_8, M_9 and M_{10}$). The result is the negative single ended term of the output current $I^{-}_{OUT}$:

$$I^{-}_{OUT} = I_{O3} + I_{O4} = \left( I^-_x I^+_w + I^+_x I^-_w \right) / I_B$$

(3.8)

Due to spread of technological parameters, each translinear loop introduces a non-linearity term $\gamma_i$ (i = 1:4). The output current can be expressed as:

$$I_{OUT} = I_{offset} + \left[ A_x x + A_w w + A_{lxy} x w \right] I_B / 4$$

where: $A_f = \gamma_1 + \gamma_2 + \gamma_3 + \gamma_4$

$$I_{offset} = \left( \gamma_1 - \gamma_2 - \gamma_3 - \gamma_4 \right) I_B / 4$$

$$A_x = \gamma_1 + \gamma_2 - \gamma_3 - \gamma_4, A_w = \gamma_1 - \gamma_2 + \gamma_3 - \gamma_4$$

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Chapter 3  Previous Architectures Related to Proposed Architecture

(a) Singe Quadrant Multiplier  (b) Block Diagram of Computational Circuit

Figure 3.3: Analog Multiplier Using Single Quadrant Multipliers [3]

The main drawback this circuit the large number of current sources used and the large aspect ratios for most of the transistors. This will increase the cost and power dissipation and degrade the bandwidth.

3.3.2 Low Voltage and Low Power Field Analog Computational Unit

The four-quadrant analog multiplier proposed in [3], can be digitally controlled to produce multiplying, squaring and inverse functions. For comparison sake only multiplying part of the work is discussed here.

The four-quadrant multiplier proposed in this work Fig.3.3a, consists of two single quadrant multipliers based on the Fig.3.3b and one current inverting circuit to produce the inverted current signals for the second multiplier.

The Transistors MP1-MP4 in Fig.3.3a form a translinear loop working in sub-threshold region. $I_1, I_2$ and are the input currents $I_3$ is the bias current and $I_4, is the output current. Using translinear principle, it is easy to show that

$$I_4 = \frac{I_1 I_2}{I_3} \quad (3.10)$$

Applying the same principle to the circuit in the Fig.3.3b, it can be seen that the signal currents $i_1$ and $I_2$, are added to the DC currents, $I_1$ and $I_2$, and the two input currents of the multiplier-1 can be written as $(I_1 + i_1)$ and $(I_2 + i_2)$, thus the output of the multiplier-1 is given by

$$I_{out1} = \frac{(I_1 + i_1)(I_2 + i_2)}{I_3} = \frac{I_1 I_2 + I_1 i_2 + i_1 I_2 + i_1 i_2}{I_3} \quad (3.11)$$

The output of the multiplier-2 is similar, with only difference being the inversion of $i_1$ and $i_2$

$$I_{out2} = \frac{(I_1 - i_1)(I_2 - i_2)}{I_3} = \frac{I_1 I_2 - i_1 i_2 - i_1 I_2 + i_1 i_2}{I_3} \quad (3.12)$$

The output current of the whole multiplier is the sum of the two single-quadrant multipliers and is given by

$$I_{out} = \frac{2I_1 I_2}{I_3} + \frac{2i_1 i_2}{I_3} \quad (3.13)$$

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Equation 3.13 implements the functions of multiplying, squaring, dividing and inversing. These functions can be controlled using external digital circuit to select one function at a time. Moreover, if operations are to be performed on DC currents only, then AC components must be set to zero and vice versa. These features are attractive for analog signal processing applications. If only the AC component is required, then a DC current component of $\frac{2I_1 I_2}{I_3}$, can be subtracted from the output current and an output current will be proportional to the multiplication of two AC input currents $i_1$ and $i_2$. The DC current $I_3$ in (3.14) can be used to scale the output.

$$I_{out} = 2 \frac{I_3}{I_1 I_2}$$

(3.14)

### 3.3.3 High Linear Four Quadrant Multiplier

This model from [4], is based on Fig.3.5, from which it is evident that the figure has two translinear loops; one is $M_1, M_2, M_3$ and $M_4$ and the other one is $M_1, M_2, M_5$ and $M_6$. If
Chapter 3

Previous Architectures Related to Proposed Architecture

Figure 3.6: Complete Circuit Schematics of Fig.3.5 [4]

The currents $I_{x1}, I_{x2}, I_{y1}$ and $I_{y2}$, from the Fig.3.5 are defined as

\[
I_{x1} = I_B + i_x \\
I_{x2} = I_B - i_x \\
I_{y1} = I_B + i_y \\
I_{y2} = I_B - i_y
\]

where $I_B$ is the bias current, $i_x$ and $i_y$ are signal currents and if the transistors in the translinear loops are operated in weak inversion region, then the output current will be

\[
I_{out} = \frac{2i_xi_y}{I_B} (3.15)
\]

Fig.3.6 [40] shows the complete schematics of Fig.3.5. The current mirror is added to Fig.3.5 in order to supply the bias current $I_B$. As shown in this circuit, many current mirrors are used. Therefore, we should pay attention to the effect by the $I_B$ mismatch because it is well-known that the device mismatches of the MOSFET’s biased in the weak-inversion region is relatively large. Because $I_{y1}$ and $I_{y2}$ maintain the differential balance in the circuit shown in Fig.3.6, the linearity of $I_{out}$ is not degraded. However, there is no balance $I_{x1}$ and $I_{x2}$. Therefore, $I_B$ mismatches for $I_{x1}$ and $I_{x2}$ degrade the linearity.

The proposed work in [4] improves the above-mentioned problem of linearity degradation by using the adaptive bias technique. Fig.3.7 shows the proposed multiplier. The difference between Fig.3.6 and Fig.3.7 is the circuit configuration for the current source $M_{xa}$ and $M_{xb}$ (see the dashed line in Fig.3.7). In Fig.3.6, sum of drain currents of $M_{1}$ and $M_{2}$ is not always equal to the tail current source ($2I_B$) because of the device mismatches in the current mirrors. Therefore, the bias current mismatches degrade the linearity of the multiplier.

On the other hand, the circuit in Fig.3.7, was designed using the adaptive bias technique for the tail current source. Using this circuit configuration, the tail current source is $I_{x1} + I_{x2}$, therefore, sum of sum of drain currents of $M_{1}$ and $M_{2}$. The input range can be tuned by $I_b$. 

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Figure 3.7: Circuit Schematics Proposed in [4]
Chapter 4

Proposed Architecture

4.1 Multiplier Architecture

The proposed multiplier circuit is shown in Fig.4.1. As can be seen from Fig.4.1, multiplication operation is done by three squarer blocks. $I_{out}$ is the output current of multiplier. $I_B$ is DC bias current. $I_x, I_y$, and $I_x + I_y$ are the input currents of squarer1, squarer2 and squarer3 respectively. $I_{in1}$ and $I_{in2}$ are extracted from the first two squarers. Then, they are added to make the input current of the third squarer cell. Output current of the multiplier can be shown to be

$$I_{out} = \frac{I_{in1}I_{in2}}{2I_B}$$  

(4.1)

4.2 Squarer Circuit

In weak inversion region, MOS current can be written as follows [41]:

$$I_D = \frac{W}{L} I_{D0} e^{\frac{V_{GS}}{V_{TH}}}$$  

(4.2)

Figure 4.1: Block Diagram of the Proposed Multiplier
where $I_{D0} = I_s \exp \frac{V_{th}}{V_{GS}}$, $I_s = 2\eta \mu C_{ox} V_T^2$, $V_T = \frac{kT}{q}$ and $\eta > 1$ is a non-ideality factor. Except for $\eta$, is similar to the exponential $I_C/V_{BE}$ relationship in a bipolar transistor. With typical values of $\eta$ and at room temperature, $I_D$ reduces by approximately a factor of 10 for every $80\text{mV}$ drop in $V_{GS}$ [41]. Fig.4.2 shows the squarer cell used in the proposed multiplier. In Fig.4.2, $I_B, I_{in}, I_3$, and $I_4$ are DC bias, input current and output currents, respectively. Since $M1$-$M4$ form a translinear loop, we can write the following equations for such a loop [42]:

$$\sum_{i=1}^{2} I_{V_{GSi}} = \sum_{i=3}^{4} I_{V_{GSi}}$$

Assuming $\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_4$ and $\left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_3$, $I_1, I_2 = I_3, I_4$. From Fig.4.2, $I_1 = I_2 = I_B$ and $I_4 = I_{in} + I_3$. Thus,

$$I_3^2 + I_{in}I_3 - I_B^2 = 0$$

$$\Rightarrow I_3 = -\frac{1}{2} I_{in} + I_B \left(1 + \frac{I_{in}^2}{4I_B^2}\right)^{\frac{1}{2}}$$

Applying power series approximation $\left((1 + x)^{\frac{1}{2}} \approx 1 + \frac{1}{2} x, -1 \leq x \leq 1\right)$ on (4.5) results in

$$I_3 = I_6 = I_7 = -\frac{1}{2} I_{in} + I_B + \frac{I_{in}^2}{8I_B}$$

$$I_4 = I_9 = I_{10} = I_{12} = \frac{1}{2} I_{in} + I_B + \frac{I_{in}^2}{8I_B}$$

$$I_{out2} = I_7 + I_{12} - I_7, I_{out1} = I_6 - I_9$$
According to power series approximation and (4.5), \( x = \frac{I^2_{in}}{I_B} \). Therefore, the above results hold for \(-2I_B \leq I_{in} \leq 2I_B\). Using (4.6) and \( I_{17} = 2I_B \), it can be shown that \( I_{out2} = \frac{I_{in}^2}{4I_B} \) and \( I_{out1} = I_{in} \). It should be noted that \( n \) has been applied in naming the nodes in Fig. 4.2 due to the fact that three squarer cells are used to build the multiplier circuit. Therefore, we use 1, 2, and 3 instead of \( n \) in the figure showing the full circuit diagram of the multiplier (see Fig. 4.4).

### 4.3 Multiplier Circuit

Fig. 4.4 shows the proposed multiplier which is made by combining three squarer cells (see Fig. 4.1). As mentioned in the previous sections, the proposed multiplier consists of 3 squarer cells and is based on Fig. 4.1. Thus, there will be 3 translinear loops consisting of M1-M2 and M3-M4 for the first loop, M1-M2 and M5-M6 for the second loop, and finally M1-M2 and M7-M8 for the third loop. According to Fig. 4.4, M3, M4, M11, output circuit 1 block, and shared circuit in green make the first squarer. Also, M5, M6, M12, output circuit 2 block, and shared circuit in green make the second squarer. Similarly, M7, M8, M13, output circuit 3 block, and shared circuit in green make the third squarer. The currents of M11, M12, and M13 are equal to \( I_B \) which is the bias current. \( I_{out2,1} \) and \( I_{out2,2} \) are equal to \( I_{in1}^2/4I_B \) and \( I_{in2}^2/4I_B \) respectively. As the input current of the third squarer cell is \( I_{out1} + I_{out1,2} = I_{in1} + I_{in2} \), then the output current of this cell will be equal to \((I_{in1} + I_{in2})^2/4I_B\). Also, \( I_{out2,1} \) and \( I_{out2,2} \) are added to form \( (I_{in1}^2 + I_{in2}^2)/4I_B \). Therefore, the output of the multiplier can be written as follows (see Fig. 4.1 and Fig. 4.4):

\[
I_{out} = I_{out2,3} - I_{out2,1} - I_{out2,2} = \frac{I_{in1}I_{in2}}{2I_b}
\]  

\( (4.7) \)
Figure 4.4: Complete Circuit of the Multiplier

Figure 4.5: Layout of Multiplier in TSMC 65nm
Chapter 4  Transconductance Mismatch

From Fig.4.1 and Fig.4.4, currents $I_{in1}, I_{in2},$ and $I_{in1} + I_{in2}$ are the inputs of squarer cell1, squarer cell2, and squarer cell3, respectively. Then, the range of $I_{in1}$ and $I_{in2}$ can be written as

$$|I_{in1} + I_{in2}| \leq 2I_B \Rightarrow |I_{in1}| \leq I_B, |I_{in2}| \leq I_b$$

Thus, the input signal range can be written as $|I_{in1,2}| \leq I_B$

4.4 Transconductance Mismatch

The effect of transconductance mismatch between NMOS and PMOS transistors in design can be modeled by rewriting (4.3) as shown below

$$\eta V_l \ln \left( \frac{I_1 (1 + \frac{\delta}{2})}{K_{p_{mos}}} \right) + \eta V_l \ln \left( \frac{I_2 (1 - \frac{\delta}{2})}{K_{p_{mos}}} \right) = \eta V_l \ln \left( \frac{I_3 (1 - \frac{\delta}{2})}{K_{p_{mos}}} \right) + \eta V_l \ln \left( \frac{I_4 (1 + \frac{\delta}{2})}{K_{p_{mos}}} \right)$$

$$\rightarrow I_1 I_2 = I_3 I_4$$

where $K_{p_{mos}} = \frac{W}{L} I_{D0} \left(1 + \frac{\delta}{2}\right)$, $K_{n_{mos}} = \frac{W}{L} I_{D0} \left(1 - \frac{\delta}{2}\right)$ and $\delta \ll 1$ is the mismatch between NMOS and PMOS transistors. It can be seen from (4.9) that mismatch between NMOS and PMOS transistors does not affect the multiplier.

4.5 Simulation Results

The proposed multiplier circuit has been designed in 65nm CMOS technology. The supply voltage and power dissipation(0,5),(997,993)
Table 4.1 shows the variation of THD and bandwidth across the different process corners. The SF corner results in the worst-case THD of 1.71% and bandwidth of 3.1MHz.

<table>
<thead>
<tr>
<th>Corner</th>
<th>THD(%) @ 100KHz</th>
<th>Bandwidth(MHz)</th>
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<tr>
<td>TT</td>
<td>1.12</td>
<td>3.5</td>
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<tr>
<td>FF</td>
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Table 4.1: THD AND BANDWIDTH IN DIFFERENT CORNERS

Fig.4.8a shows monte-carlo analysis when the inputs have their maximum values equal to 200nA, across 50 different process and mismatch corners. The mean value and standard deviation are 99.5nA and 1.5nA, respectively. Low sensitivity of the proposed circuit to technology process variations is observable for the responses. In addition, monte carlo simulation is done for THD and bandwidth of the circuit for more robustness evaluation of the multiplier against fabrication process uncertainties. Fig.4.8b shows the histogram of THD across different process and mismatch corners. The mean value and standard deviation of THD are 1.42% and 0.33% respectively. Fig.4.9a shows the histogram of bandwidth across different process and mismatch corners. Fig.4.9a indicates the mean value and standard deviation of the bandwidth are 3.3MHz and 0.24MHz respectively.

In Fig.4.9b, the effect of temperature for the circuit has been investigated from −20 to 100°C. According to this figure, the second input is constant, $I_{in2} = 100nA$, and $I_{in1}$ varies in the range of $-200nA \leq I_{in1} \leq 200nA$. This figure shows that current variation is less than 2%. Table 4.2 shows a comparison between this work and the other reported current mode analog multipliers including transistors working in weak inversion.
Chapter 4 Simulation Results

(a) Monte Carlo analysis when both inputs have their maximum values which are 200nA and the output current is 100nA

(b) Monte Carlo analysis result of the multiplier for THD

Figure 4.8: Total Harmonic Distortion Analysis

(a) Monte Carlo analysis result of the multiplier for bandwidth

(b) Output current versus temperature under the condition that $I_{in2} = 100nA$ and $I_{in1}$ is between ±200

Figure 4.9: Monte Carlo for Bandwidth and Temperature Analysis of $I_{out}$
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<tr>
<th>Parameters</th>
<th>[2]</th>
<th>[3]</th>
<th>[43]</th>
<th>[4]</th>
<th>[44]</th>
<th>[45]</th>
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<td>±200</td>
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Table 4.2: COMPARISON
Bibliography


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